High-Performance Printed Transistors Realized Using Femtoliter Gravure-Printed Sub-10 μm Metallic Nanoparticle Patterns and Highly Uniform Polymer Dielectric and Semiconductor Layers

*Hongki Kang, Rungrot Kitsomboonloha, Jaewon Jang, and Vivek Subramanian**

Printed electronics has received a great deal of attention as a means of realizing a wide range of low-cost printed electronic systems. High-speed roll-based printing is particularly attractive due to its potential for very high throughput and low cost of ownership. As a result, there have been several attempts by numerous groups including our own to use various types of roll-to-roll printing, such as direct gravure printing, off-set printing, and flexographic printing to fabricate printed transistors.[1–6] Unfortunately, to date, the performance of such thin-film transistors (TFTs) has been limited by the large dimensions of such printed devices (typically gravure printing produces features >50 μm), the low mobility of the printed semiconductors, and the poor electrostatic integrity of the realized devices, resulting in poor operating frequencies of demonstrated ring oscillators, ≈2.5 to 150 Hz[1,4,5] and high operating voltages in the range of ≈50 to 100 V.[1–6] To make printed electronics a reality, is it critical that orders of magnitude better performance be achieved. For example, radio frequency identification (RFID) tags require data rates in the range of 100 kHz or more, as do fully integrated displays. Additionally, the systems of interest require operation at voltages of <20 V.

One important figure of merit for the performance of transistors is the transition frequency, f_T as shown in Equation (1) in saturation mode, at which an unloaded transistor shows unity current gain.

$$f_T = \frac{\mu V_{DS,SAT}}{2\pi L^2 \alpha} \quad (1)$$

where L is channel length, μ is field-effect mobility, $V_{DS,SAT}$ is the voltage between the drain and source in saturation mode, and α is a constant determined by the operating region and the overlap between the gate and the source/drain electrodes (hereafter referred to as gate overlap). Typically, f_T represents an upper limit of performance. Examining the equation above, for higher performance devices, it is necessary to scale channel length, minimize parasitic losses, and keep the operating voltage as high as possible within an application-determined acceptable range.[7] A tremendous body of knowledge exists to drive the improvement in the field-effect mobility of printed organic semiconductors.[8,9] The benefits of scaling organic transistors to channel lengths below 10 μm to achieve MHz operation have also been demonstrated, but these small channel lengths were only obtained via photolithography.[10–12] Unfortunately, on the other hand, very little work has been performed to properly scale the channel length of printed TFTs, including development of printing techniques and realization of suitably designed materials and ink formulations. Although there have been some demonstrations of devices with reduced channel lengths by reducing the spacing between the printed source and drain, the performance of these demonstrations was limited by the large overlap capacitances resulting from the large dimensions of the gate electrode.[3,5] Therefore, in order to fully benefit from the reduction of channel length for better AC characteristics, it is vital to reduce the width of the conductive electrodes regardless of the device structure used. As an example of this, Sekitani et al. demonstrated transistors with channel lengths as small as 2 μm by utilizing sub-femtoliter inkjet-printed droplets.[13] However, as inkjet printing is scaled to finer drops, printing speeds slows unacceptably since the number of drops required to build a pattern increases in correspondence to the reduction in drop size. Furthermore, multiple inkjet passes are required to make lines conductive due to the low metal content, which lowers throughput even more. As a result, while femtoliter inkjet printing allows for pattern scaling, the associated materials and process limitations make the viability of this technique questionable.

Here, we demonstrate high-performance printed TFTs, scaling to unprecedented levels via advanced femtoliter-scale micro-gravure printing (μGravure), to realize devices with excellent DC and AC characteristics. This is achieved through a combination of novel and dramatically improved gravure printing processes, properly optimized and characterized materials, and proper electrostatic scaling. By proper scaling, we achieve record transition frequencies of >300 kHz, and >1000× improvement over other work. We are able to print sheets of devices at printing speeds of almost 1 m s^{-1}, an important step in the development of truly low-cost fabrication processes.

H. Kang, R. Kitsomboonloha, J. Jang, V. Subramanian
Department of Electrical Engineering and Computer Sciences, University of California Berkeley, Berkeley, CA 94720-1770, USA
E-mail: viveks@eecs.berkeley.edu
Prof. V. Subramanian
World Class University Program
Sunchon National University
413 Jungangro (315 Maegok), Suncheon, Jeonnam, 540-742, South Korea

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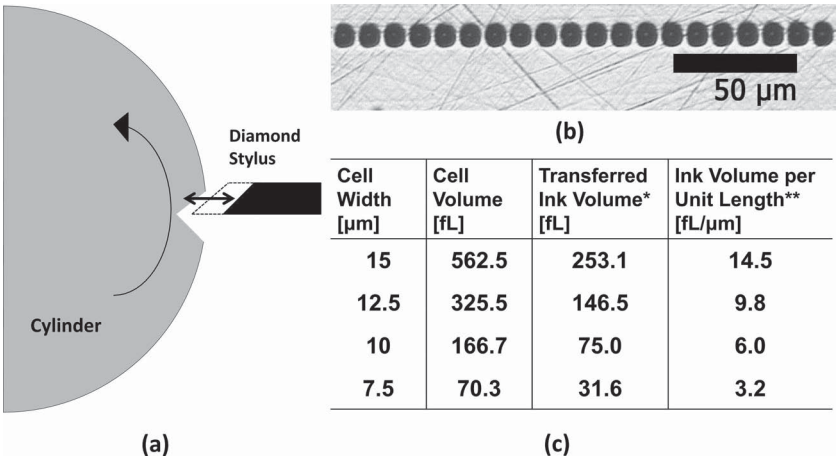

Cell Width [μm]	Cell Volume [fL]	Transferred Ink Volume* [fL]	Ink Volume per Unit Length** [fL/μm]
15	562.5	253.1	14.5
12.5	325.5	146.5	9.8
10	166.7	75.0	6.0
7.5	70.3	31.6	3.2

Figure 1. a) Electromechanical engraving. b) Electromechanically engraved 7.5 μm wide gravure pattern cells (pyramidal shape, depth = 0.5 width) with 2.5 μm spacing. c) Properties of engraved pyramidal cells on the gravure roll. The cell width is the side length of a square base of the pyramid. The ratio of cell width to depth is determined to be 2 by the shape of the diamond stylus used for engraving. *The volume of transferred ink onto the substrate is about 45% of the volume of the engraved cells; see Supporting Information). **Values are calculated assuming the spacing between cells to be 2.5 μm.

Gravure printing uses a roll-based master to transfer patterns onto flexible substrates at high-speed. High pattern fidelity is achieved by using precisely defined well shapes on the master along with appropriately formulated inks and printing conditions. In order to realize sub-10 μm patterns on the master with low variation and excellent fidelity, highly scaled gravure printing masters were produced using a novel electromechanical engraving process (**Figure 1**a) in which a pyramidal diamond stylus tip moves in and out of a copper gravure roll that rotates to create a digitally-defined pattern. Because of significant hardness difference between the stylus and the master roll, minimized cell-to-cell variation (Figure 1b) is obtained with the electromechanical engraving compared to chemical etching techniques, which suffer more from non-uniformity due to inconsistent etch rate and directionality. The smallest achieved pattern is a pyramid with a 7.5 μm wide square base and 3.75 μm depth. This is an order of magnitude smaller than conventional graphic art gravure printing cells (≈50 to 200 μm wide cells). As shown in Figure 1c, the volume of transferred ink from a single pyramidal cell is decreased cubically as we reduce the size of the cells. Since not all the ink filled in the cell is transferred to the substrate during printing, the actual ink volume from the smallest 7.5 μm cell is only approximately 32 fL, which is more than an order of magnitude smaller than the typical volume of a single inkjet-printed drop, 1–10 pL. During the printing of uniform lines, the width is determined by the printed ink volume per unit length, as in Equation (2).

$$\text{Line Width} = \sqrt{\frac{8\sin^2\theta}{2\theta - \sin 2\theta}}\sqrt{V_{\text{per length}}} \quad (2)$$

where θ is the equilibrium contact angle and $V_{\text{per length}}$ is the volume of the transferred ink per unit length.[14,15] Comparing the μGravure technique herein (3.2 fL μm^{-1}) with state-of-the-art sub-femtoliter inkjet printer (0.7 fL per ≈1 to 2 μm),[13] establishes that there is less than an order of magnitude difference between the two. Simultaneously, μGravure allows for dramatically improved throughput (many orders of magnitude) and film build-up.

Thus, this technique allows for very aggressive dimensional scaling of printed features while maintaining very high printing speeds (≈1 to 10 m s^{-1}), independent of feature scaling, unlike inkjet printing. Therefore, μGravure printing is a very promising technology for the scaling of features in a viable and controllable manner.

The printing process physics and consequently, the pattern generation, of gravure printing is fundamentally much more complicated than inkjet printing system because of the nature of contact printing. Therefore, it is vital to understand how rheological parameters of the inks affect the patterns produced by the μGravure printing. This knowledge can establish a basis for future μGravure printable active ink development for dielectric, conductive, and semiconducting materials. This is especially important for the printing of highly scaled lines as required in scaled printed transistors since any small defect or pinhole can cause catastrophic process failure and device death. Although there are many established models available for the estimation of inkjet-printed features, very little work has been performed on the modeling and characterization of gravure printing.[14–16]

Dielectric layer integrity is a critical parameter for the realization of printed transistors. Therefore, using a widely used polymer dielectric, poly-4-vinylphenol (PVP) dissolved in 1-hexanol, we studied the impact of ink viscosity and printing speed on the completeness of pattern formation, with a particular focus on pinhole formation, a critical factor for dielectric printing. PVP is attractive as a model system because of its simple solvent system and viscosity controllability.[15,16] The viscosity of this shear-thinning polymer ink can be easily varied from 10 cP to 500 cP by adjusting polymer concentration. As shown in **Figure 2**a, as the viscosity of the ink increases, more complete square features are printed. The use of inks having very low viscosity (≈10 cP) leads to poor ink transfer, resulting in significant film break-up. On the other hand, inks with higher viscosities of ≈100 cP often produce complete squares with well defined edges and no pinholes.

Printing velocity also has a significant effect on the pattern formed by a given ink. As shown in Figure 2b, for a fixed ink, incomplete dots are printed when printed at low speed compared to well-formed circular dots realized during high-speed printing. High viscosity and high printing speed both lead to the increase of capillary number of the ink. Thus, it is found that relatively high capillary number is required to improve the printability of the inks in μGravure printing. The same behavior is also observed in more complex systems. When a silver nanoparticle ink with viscosity of ≈100 cP is used to print lines at different printing speeds, the low-speed printed lines show significant pinholes along the line as shown in Figure 2c. The

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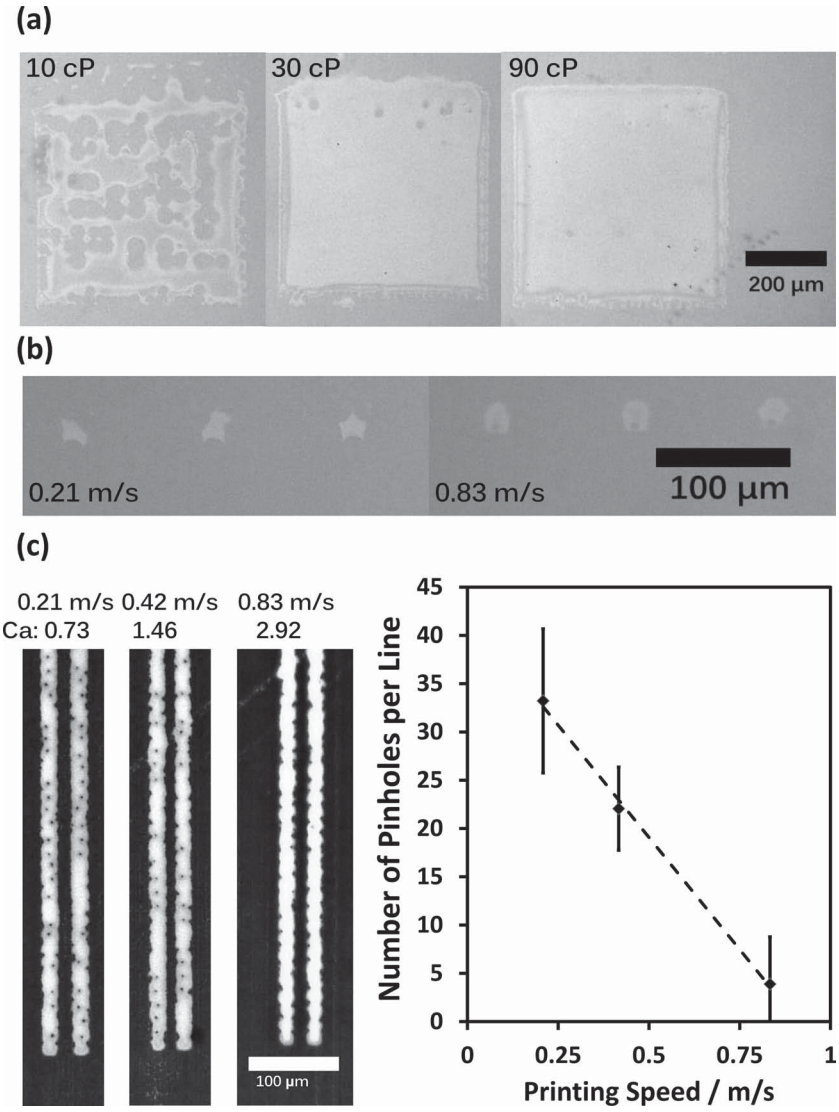

Figure 2. a) µGravure printed 500 µm squares of PVP printed from an array of 15 µm wide cells with 2.5 µm cell spacing. The viscosity of the inks is varied from 10 cP to 90 cP. b) Individual dots of PVP from 15 µm wide cells are printed at different printing speeds. The viscosity of the PVP ink is 90 cP. c) Gravure printed 5 nm silver nanoparticle ink at different printing speeds. Viscosity of the ink is 100 cP and the cells are 12.5 µm wide with 2.5 µm spacing. The capillary number is calculated from the viscosity and printing speed; the accuracy of this value is limited by shear-thinning effects in the ink at high speeds. Average number of pinholes per a 900 µm long line is measured from 16 printed lines printed at different printing speeds.

number of pinholes decreases as the printing speed increases. High viscosity and high speed are often very desirable since those lead to higher mass loading and better throughput.

Printed transistors are multilayer devices, with multiple layers overlaid onto each other. Therefore, the 3D morphology of printed lines is of critical importance in device formation. For example, the thickness of conductive lines determines the resistance of the same, which can limit circuit operating speed. Additionally, the smoothness of printed conductive lines is critical for their use as bottom gates in transistors because rough underlying gates will tend to cause defects such as pinholes in overlying gate dielectric layers. The surface roughness of the gate line in bottom gate OTFTs affects not only the leakage current and breakdown characteristics of the dielectric layer, but also the mobility of the semiconductor.[17] Therefore, in addition to the dielectric study above, to allow for proper materials and process optimization, we study the materials-process-structural relationships of printed conductive lines. Conducting polymers such as poly(3,4-ethylene dioxythiophene) doped with poly(styrene sulfonate) (PEDOT:PSS) have been previously printed with roll-to-roll printers.[1,3–5] However, the resistance of this conducting polymer is unacceptably high for use in high-speed circuits. To overcome this, we have previously studied the use of an organometallic silver precursor ink.[6] However, the low metal content (≈10 wt%) of this system limits scalability due to absence of conductive paths for thin films and also due to enhanced pattern spreading due to the low viscosity of the ink. To overcome these limitations, in this work, we study the gravure printing of highly scaled lines based on metallic nanoparticles.

Particle size is clearly a key parameter in formation of lines based on printed nanoparticles. We study the printing of two nanoparticle-based metal inks with different particle sizes. Both inks have high metal contents above 50 wt%. Even though the two inks are able to produce sub-10 µm wide lines with reasonable thickness (35–60 nm), the characteristics of the lines are quite different depending on the size of the nanoparticles. Although the ink containing 50 nm Ag nanoparticles prints thicker lines, the lines become very resistive as feature sizes are scaled below 10 µm due to the loss of continuous conduction paths. As the thickness of the lines approaches the nanoparticle diameter, a near-monolayer printed structure results, preventing the formation of good conductive percolative networks. Additionally, the surface roughness of 50 nm nanoparticle lines is significantly higher due to the large size of the particles as shown in **Figure 3**. On the other hand, 5 nm gold nanoparticle based ink leads to much better conductivity in spite of reduced film thickness, and much improved surface roughness (RMS 2.31 nm). The improvement in conductivity can be attributed to the densely packed structure, offering well-connected paths for percolation-based conduction. The low surface roughness improves the endurance of dielectric layer built upon the metal lines. PVP capacitors printed on the metal lines show very low leakage current density, 1 µA cm^{-2} at 2 MV cm^{-1} when PVP layer thickness is also significantly scaled (see Supporting Information).

Highly scaled µGravure-printed lines based on the optimized ink properties above show good scalability and controllability.

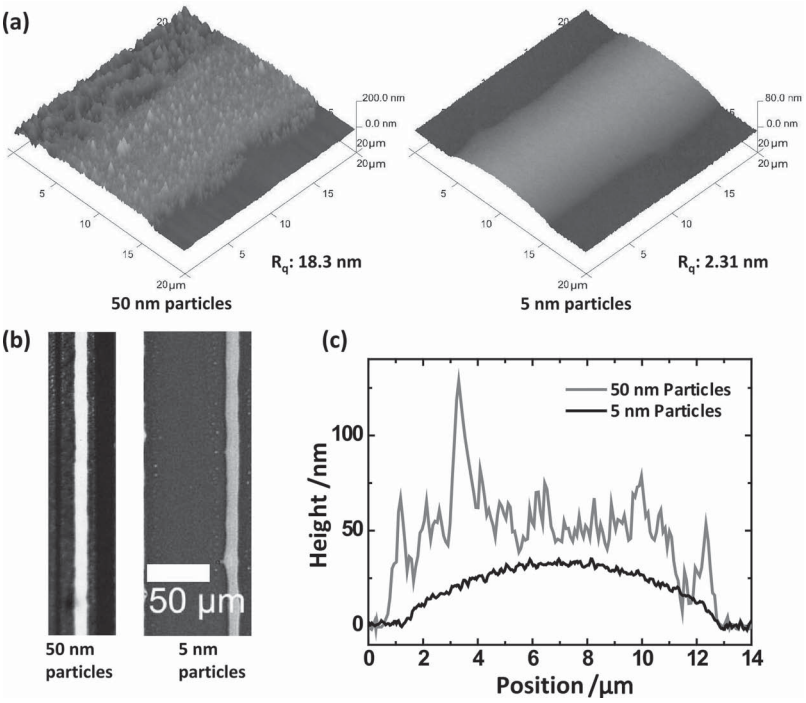

Figure 3. a) AFM images of gravure printed metal lines with different nanoparticle sizes (50 nm size silver nanoparticles, 5 nm size gold nanoparticles).The scan area is 20 μm × 20 μm. RMS roughness of the lines (R_q) is provided. b) Optical images of the gravure printed metal lines (from 10 μm square cells with 3.75 μm cell spacing), showing excellent pattern fidelity. c) Surface profile of the printed metal lines.

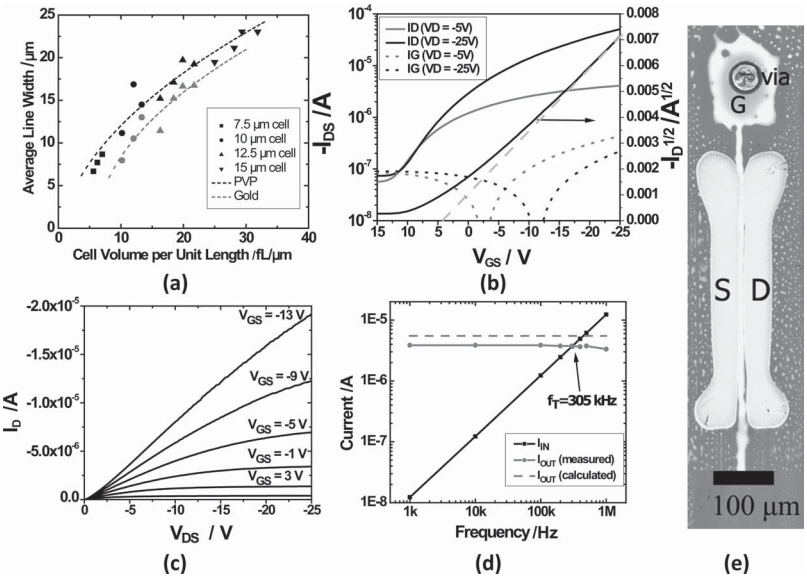

Figure 4. a) Scaling of gravure printed lines on PEN (PVP lines: black symbols, and gold lines: gray symbols). μGravure cell sizes ranged from 7.5 μm to 15 μm with four different spacing from 2.5 μm to 7.5 μm. Both showed theoretical relationship between the width and volume of lines; width is proportional to (volume)$^{0.5}$. Fitting lines are plotted alongside data symbols to show quality of fit. b) Transfer and c) output characteristics of a representative highly scaled μGravure-printed TFT with $\mu_{LIN} = 0.025$ cm^2 V^{-1} s^{-1}, $\mu_{SAT} = 0.105$ cm^2 V^{-1} s^{-1}. d) AC characteristics of the representative TFT. Dashed line indicates theoretically calculated output current based on measured transconductance, load resistance, and input signal, showing good agreement with the experimentally observed data. (grey dashed line). e) Optical microscopy image of the representative pBTTT TFT ($W = 416$ μm, $L_{channel} = 10$ μm with minimal gate overlap).

As shown in **Figure 4**a, changing the size and spacing of gravure cells enables reduction of the width of μGravure-printed polymer and metal lines down to 6.3 μm with line edge roughness (LER) as low as 2 μm. This excellent LER allows for the realization of very tight gaps between adjacent printed lines. Measured width of the gravure printed lines is in good agreement with the hydrostatically determined theoretical relationship in Equation (2). Good accordance with the equation proves good controllability of our printing process. Highly scaled metal lines still deliver low sheet resistance of about 20 Ω per □, which is several orders of magnitude lower than commonly gravure printed PEDOT:PSS lines[5] and is more than adequate for use in OTFT electrodes.

Given the high quality and scalability of the μGravure printed lines above, we proceed to demonstrate their integration into high-performance bottom-gate gravure-printed OTFTs, formed on commercial planarized polyethylene napthalate (PEN) substrates. A process flow for the various layers is adopted from ref. [6] with further scaling of the relevant conductor and dielectric layers as discussed above. (See more detail in the experimental section.) poly(2,5-bis(3-alkythiophen-2-yl)thieno[3,2-b]thiophene), also widely known as pBTTT, supplied by EMD Chemicals, was used as the semiconductor. Transfer and output characteristics of the pBTTT TFTs are shown in Figure 4b,c. The device has a channel length of 10 μm with almost no gate overlap, showing the excellent performance of the overall gravure printing process. The device has a reasonably high mobility of about 0.1 cm^2 V^{-1} s^{-1}, which approaches the highest literature-reported values for this semiconductor. This excellent performance is attributed to the smooth interface resulting from properly optimized smooth gate metal lines.[17] The pBTTT TFTs in this work have ten times higher mobility and two times smaller channel length than our previous work; simultaneously the operating voltage has been significantly reduced.[6] To demonstrate the benefits of the highly-scaled devices herein, the transition frequency (f_T) of the pBTTT devices was measured. As shown in Figure 4d, the transition frequency when the TFTs were biased at V_{GS} = –19 V and V_{DS} = –20 V was measured to be 305 kHz, which is by far the highest switching speed reported to date for any roll-printed process while biased at lowest voltages.

In summary, highly scaled, 10 μm channel length, bottom-gate organic TFTs were fabricated on flexible plastic substrates using a novel large-area femtoliter-scale microgravure printing process at a high printing speed (0.83 m s^{-1}) with a pBTTT semiconductor. The resulting

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devices showed excellent performance, with the highest transition frequency reported to date for any roll-printed device. Transition frequencies of 300 kHz were obtained at operating voltages of 20 V; this switching performance is likely adequate for a wide range of flexible electroncis applications, and thus, we demonstrate the clear benefits of proper materials optimization and electrostatic scaling in conjunction with advanced printing to realize high-performance printed transistors.

Experimental Section

Printed Inks: PVP inks with different viscosities were formulated and used in this study. Inks with PVP wt% of 7.6, 14.1 and 19.8 respectively had viscosities of 10, 30, and 90 cP. The PVP inks were formulated using poly-4-vinylphenol (PVP) ($M_w \approx 11\,000$ from Sigma Aldrich) dissolved in 1-hexanol (99.0%, from Sigma Aldrich). As discussed above, various conductive inks were used in this work. For organometallic ink printing, Inktec PR-010 silver precursor ink was used. A silver nanoparticle ink with a 50 nm nanoparticle size, DGP, was purchased from Advanced Nano Products (ANP). The metal content of the ink was 75 wt% as received with a viscosity of 100 P; this was diluted to tune the viscosity of the ink by addition of isopropyl alcohol while maintaining the metal content above 50 wt%. A gold nanoparticle ink, NPG-J, was purchased from Harima Chemicals. This ink had an average particle size of 5 nm. In spite of its low viscosity (≈10 cP), it had a high metal content of ≈50 wt% and showed excellent printability in our gravure process.

Fabrication Process, Transistor Structure, and Characterization: Transistors were printed on planarized polyethylene napthalate (PEN) substrates provided by DuPont Teijin Films. This substrate was selected due to its good thermal stability and wide contact angle hysteresis due to near zero receding contact angle. It was previously shown that low receding contact angle minimizes de-wetting of printed 1D and 2D features, resulting in more complete features.[14–16] Thus, the small receding contact angle of the planarized PEN substrate used in this work helped ensure completeness of gravure printed patterns.

To realize bottom-gate TFTs on PEN, gold gate lines and PVP dielectric layers (160 nm thick) were gravure-printed as above. It was necessary to have minimized gate overlap to ensure good AC characteristics. Though significant effort has been devoted to improve the layer-to-layer alignment of roll-to-roll printing processes, the overlay printing registration accuracy of these processes was still typically worse than 15 µm, which was not adequate for OTFTs with 10 µm channel length.[18] Therefore, in this work, silver source and drain electrodes were deposited by inkjet printing (Cabot CCI-300 nanoparticle silver ink); note that inkjet printing can be easily integrated into roll-to-roll processes and can be combined with high-speed gravure printing to realize high-speed overall layer printing. To achieve maximized throughput in this regard, it was also necessary to optimize sintering conditions using appropriate materials to realize roll-to-roll compatible sintering times.[19,20] As a last step, an organic semiconductor, poly(2,5-bis(3-alkythiophen-2-yl)thieno[3,2-b] thiophene) also widely known as pBTTT, supplied by EMD Chemicals, was spin-coated and annealed for 10 min at 160 °C under nitrogen. pBTTT is advantageous for this application since it was previously shown to be gravure-printable with good stability and uniformity.[6] Because pBTTT forms an isotropic liquid crystal when annealed above a certain temperature, uniform heating provided uniform crystalline structure of the semiconductor, resulting in minimized device-to-device variation. The detailed fabrication process and device structure are shown in the Supporting Information.

Fabricated OTFTs were characterized under nitrogen to minimize any effect of oxygen and moisture, although pBTTT was previously shown to be reasonably air stable. In the future, gravure printing can also be used to print encapsulation. DC characteristics were measured using an Agilent 4156C semiconductor parameter analyzer. A standard f_T measurement setup was used with a high impedance active probe, Picoprobe Model 18C with 20 fF input capacitance by GGB Industries Inc. to minimize coupling.

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